In the Claims:

1. (Previously Presented) A method of forming post passivation interconnects for an integrated circuit having a first plurality of contact pads in a first connection pattern, the method comprising:

forming a passivation layer over the integrated circuit and over the first plurality of contact pads, wherein the first plurality of contact pads could otherwise be used to provide electrical connection to an external component in packaging the integrated circuit by the formation of wire bonds or solder balls on the first plurality of contact pads, the passivation layer being formed from a non-oxide material;

forming a buffer layer over the passivation layer, the buffer layer comprising a silicon oxide layer;

removing a top portion of the buffer layer;

depositing a post passivation metal layer over the buffer layer after removing a top portion of the buffer layer;

forming a second connection pattern in the post passivation metal layer such that portions of the second connection pattern are electrically coupled to the first plurality of contact pads, wherein the second connection pattern differs from the first connection pattern; and

forming a second plurality of contact pads while forming the second connection pattern and as part of the second connection pattern.

2. (Original) The method of claim 1 wherein the top portion of the buffer layer is removed in a cleaning chamber having an inner wall comprising primarily quartz.

3. (Original) The method of claim 2 wherein the cleaning chamber is in a vacuum condition during the removing step and wherein the post passivation metal layer is deposited over the buffer layer after the removing step without breaking the vacuum condition in the cleaning chamber.

4. (Original) The method of claim 1 wherein passivation layer is formed in a first chamber that is in a vacuum condition and wherein the buffer layer is formed over the passivation layer in the first chamber and without breaking the vacuum condition in the first chamber after forming the passivation layer.

5. (Original) The method of claim 4 wherein the top portion of the buffer layer is removed in the first chamber, the method further comprising breaking a vacuum condition in the first chamber before the step of etching the buffer layer.

6. (Original) The method of claim 1 wherein the passivation layer comprises a layer of silicon nitride.

7. (Original) The method of claim 1 wherein the passivation layer comprises more than one layer and wherein an uppermost layer comprises silicon nitride.

8. (Previously Presented) The method of claim 1 wherein the buffer layer has a thickness substantially smaller than a thickness of the passivation layer and wherein the buffer layer has a thickness less than about 25 nanometers.

9. (Previously Presented) The method of claim 1 wherein the buffer layer has a thickness substantially smaller than a thickness of the passivation layer and wherein the ratio of the thickness of the passivation layer to the thickness of the buffer layer is greater than about 20.

10. (Cancelled)

11. (Previously Presented) The method of claim 34 wherein the oxide buffer layer is etched in a chamber that includes quartz inner walls.

12. (Previously Presented) The method of claim 34 wherein the thickness of the passivation layer is at least about 20 times greater than the thickness of the oxide buffer layer.

13. (Previously Presented) The method of claim 12 wherein the oxide buffer layer has a thickness of less than about 25 nm.

14-21. (Cancelled)

22. (Previously Presented) A method of forming a semiconductor device, the method comprising:

providing a silicon substrate having a plurality of active devices formed therein, the active devices being interconnected by a plurality of metal layers including an uppermost metal layer, the uppermost metal layer including a first plurality of contact pads, wherein the first plurality of contact pads could otherwise be used to provide electrical connection to an external component in packaging an integrated circuit chip comprising the semiconductor device by forming wire bonds or solder balls on the first plurality of contact pads;

forming a nitride passivation layer overlying the uppermost metal layer except for selected contact openings to the first plurality of contact pads;

forming an oxide buffer layer overlying the nitride passivation layer, the oxide buffer layer having a thickness substantially smaller than a thickness of the nitride passivation layer; and

forming a post passivation metal layer overlying the oxide buffer layer, the post passivation metal layer patterned so as to electrically couple the first plurality of contact pads to a second plurality of contact pads formed in the post passivation metal layer.

23. (Previously Presented) The method of claim 22 wherein forming a nitride passivation layer comprises forming a silicon nitride layer and wherein forming an oxide buffer layer comprises forming a silicon oxide layer.

24. (Previously Presented) The method of claim 22 wherein forming an oxide buffer layer comprises forming an oxide buffer layer with a thickness of less than 25 nanometers.

25. (Previously Presented) The method of claim 22 wherein thickness of the nitride passivation layer is at least about 20 times greater than the thickness of the oxide buffer layer.

26. (Previously Presented) The method of claim 22 wherein the first plurality of contact pads are disposed around the periphery of the chip and the second plurality of contact pads are arranged over a central portion of the chip.

27. (Previously Presented) The method of claim 22 and further comprising:

providing a package substrate having a plurality of package contact pads arranged in a configuration corresponding to the second plurality of contact pads on the chip; and

attaching the package contact pads of the package substrate to the second plurality of contact pads on the chip via a plurality of solder bumps, wherein the solder bumps electrically couple the second plurality of contact pads on the chip with the package contact pads on the package substrate.

28. (Previously Presented) The method of claim 22 wherein the uppermost metal layer comprises a layer of copper.

29. (Previously Presented) A method of forming a post passivation metal layer over an integrated circuit, the method comprising:

providing a substantially completed integrated circuit formed to the point that only connection to an external circuit would be needed to allow the device to operate, the substantially completed integrated circuit including a silicon nitride passivation layer at an uppermost surface;

forming an oxide buffer layer over and physically contacting the silicon nitride passivation layer, the oxide buffer layer having a thickness substantially smaller than a thickness of the passivation layer;

removing a top portion of the oxide buffer layer, the top portion of the buffer layer being removed in a cleaning chamber having an inner wall comprising primarily quartz, the cleaning chamber being held in a vacuum condition during the removing;

depositing a metal layer over and physically contacting the oxide buffer layer, wherein the metal layer is deposited after the removing step without breaking the vacuum condition in the cleaning chamber; and

patterning the metal layer to form a connection pattern comprising a plurality of contact pads.

30. (Previously Presented) The method of claim 29 wherein the passivation layer comprises a layer of Si_3N_4.

31. (Previously Presented) The method of claim 29 wherein the passivation layer comprises more than one layer and wherein an uppermost layer comprises silicon nitride.

32. (Previously Presented) The method of claim 29 wherein forming an oxide buffer layer comprises forming buffer layer that has a thickness of less than about 25 nanometers.

33. (Previously Presented) The method of claim 29 wherein the ratio of the thickness of the passivation layer to the thickness of the buffer layer is greater than about 20.

34. (Currently Amended) A method of forming post passivation interconnects for an integrated circuit, the method comprising:

forming a passivation layer over a substantially complete integrated circuit and over a first plurality of contact pads, the first plurality of contact pads being in a first connection pattern, wherein the passivation layer is formed from a non-oxide material;

forming an oxide buffer layer over ~~and abutting~~ the passivation ~~layer, the oxide buffer layer having a thickness substantially smaller than a thickness of the passivation~~ layer;

forming a metal layer over the oxide buffer layer; and

patterning the metal layer to form a second connection pattern comprising a second plurality of contact pads, wherein at least some of the second plurality of contact pads are electrically connected to at least some of the first plurality of contact pads, wherein at least some of the second plurality of contact pads are on a different level than the first plurality of contact pads, and wherein the second connection pattern differs from the first connection pattern.